In the Claims

Claims 55-61 and 80-82 are pending in the application with claim 55 amended herein, claims 62-68 and 79 cancelled herein, and new claims 81 and 82 added herein.

Claims 1-54 (cancelled).

55. (currently amended) An integrated circuit forming method comprising:

forming a first layer comprising copper for an integrated circuit over a substrate;

forming a second layer comprising a second metal different from copper over the first layer, the second metal comprising palladium;

incorporating at least some of the palladium into an intermetallic layer comprising ~~the palladium and~~ copper and palladium from the respective first and second layers and having a thickness of from about 50 to about 150 Angstroms;

removing at least a portion of any second metal that is not incorporated into the intermetallic layer and exposing the intermetallic layer; and

forming a conductive connection for an integrated circuit directly to the exposed intermetallic layer without a passivation layer therebetween.

56. (previously presented) The method of claim 55 wherein the intermetallic layer consists of copper and palladium.

57. (previously presented) The method of claim 55 wherein the incorporating comprises annealing the first and second layer at a temperature of greater than 400 to about 500 °C.

58. (previously presented) The method of claim 55 wherein the first layer has an elevational thickness before the incorporating, further comprising removing any second metal not comprised by the intermetallic layer, and any portion of the intermetallic layer, beyond the elevational thickness.

59. (previously presented) The method of claim 58 wherein the removing comprises chemical mechanical polishing.

60. (previously presented) The method of claim 55 wherein a rate of removing the second layer compared to the intermetallic material comprises greater than 5 to 1.

61. (previously presented) The method of claim 55 wherein the second layer consists of palladium.

Claims 62-79 (cancelled)

80. (previously presented) The method of claim 55 further comprising, after the removing, exposing the intermetallic layer to conditions effective to oxidize the first layer, but the intermetallic layer protecting underlying portions of the first layer from oxidation during the exposing.

81. (new) An integrated circuit forming method comprising:

forming a first layer comprising copper for an integrated circuit over a substrate;

forming a second layer comprising a second metal different from copper over the first layer, the second metal comprising palladium;

incorporating at least some of the palladium into an intermetallic layer consisting of copper and palladium from the respective first and second layers by annealing the first and second layers at a temperature of greater than 400 to about 500 °C, the intermetallic layer having a thickness of from about 50 to about 150 Angstroms and the copper and palladium of the intermetallic layer being held together by metallic bonding;

after the annealing, removing any second metal that is not incorporated into the intermetallic layer and exposing the intermetallic layer; and

forming a conductive connection for an integrated circuit directly to the exposed intermetallic layer without a passivation layer therebetween.

82. (new) The method of claim 81 further comprising, after the removing, exposing the intermetallic layer to conditions effective to oxidize the first layer, but the intermetallic layer protecting underlying portions of the first layer from oxidation during the exposing.